AN-5058

µSerDes™ Family Frequently Asked Questions (FAQs)

Summary

The following questions are typical of Fairchild's µSerDes™ application support team answers the µSerDes family. If you have a question not addressed here, please contact your local Fairchild representative or email to interface@fairchildsemi.com.

What is a µSerDes™?

The µSerDes is a low-cost, ultra-low EMI, very small device that allows large amounts of data to flow between points such as displays, cameras, and controllers. This is achieved through a parallel-to-serial (serializer) conversion at the source and serial-to-parallel (deserializer) conversion at the destination.

Why is a Fairchild µSerDes™ serial interface better than a parallel interface solution?

- Significantly reduced EMI over single-ended technology solutions.
- No power-up sequencing required. No change needed for controller software.
- Functions well where single-ended, current-mode technology fails.
- Can provide a greater than 25 to 4 wire reduction.
- Can provide a greater than 50 to 7 wire reduction in bi-directional interfaces.
- Can provide a lower-cost, more reliable interface solution.
- Can reduce overall component count over existing LVCMOS technology.
- Can use less board space over LVCMOS technologies.

What are the differences among the µSerDes™ devices?

Each device in the Fairchild µSerDes family has been designed for specific architectures as shown in Table 1.

Table 1. µSerDes™ Family Comparisons

	FIN12AC	FIN24AC	FIN24C	FIN212AC	FIN224AC	FIN324C
Function	Serializer / Deserializer	Serializer / Deserializer	Serializer / Deserializer	Serializer / Deserializer	Serializer / Deserializer	Serializer / Deserializer
Number of Bits	12	22	24	12	22	24
Max Frequency	40MHz	20MHz	20MHz	40MHz	26MHz	15MHz
*Factory Options (***Contact Factory)*			26MHz	*48MHz & 2.5x2.5 package*		*Higher frequency version*
Dynamic Current (Serializer)	8.5mA @ 5MHz	9.5mA @ 5MHz	11mA @ 10MHz	9.5mA @ 5MHz	9mA @ 5MHz	4mA @ 5.44MHz
VDDA/S	2.5 to 3.3V	2.5 to 2.9V	2.5 to 2.9V	2.5 to 3.6V	2.5 to 3.3V	2.5 to 3.0V
VDDP	1.65 to 3.6V	1.65 to 3.6V	1.65 to 3.6V	1.65 to 3.6V	1.65 to 3.6V	1.6 to $V_{DDA/S}$
Read / Write	Write	Write	Write	Write	Write	Read / Write
Ideal Application	Camera	Small LCD	Small LCD	Camera Small LCD	Small LCD	Small LCD
Recommended Interface	RGB	µController	RGB	µController / RGB	µController	µController / RGB / SPI
Selectable LVCMOS Edge Rates	No	No	No	Yes	Yes	Yes
Selectable LVCMOS Pulse Width	No	No	No	Yes	Yes	Yes
Output state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Known-state
External timing required	Yes	Yes	Yes	Yes	Yes	No
Additional Features	Multiple frequency range	Multiple frequency range		Multiple frequency range; CTL Standard or High;PLL divide by 2 or 3	Multiple frequency range	RT180
ESD in kV	15	8	8	14	15	15
Package	BGA, MLP	BGA, MLP	BGA, MLP	BGA, MLP	BGA, MLP	BGA, MLP
Modes	0-Power Down; 1-CKREF 20Mhz to 40MHz; 2-CKREF 5MHz to 14MHz; 3-CKREF 8MHz to 14MHz	0-Power Down; 1-CKREF 2Mhz to 5MHz; 2-CKREF 5MHz to 15MHz; 3-CKREF 10MHz to 20MHz	0-Power Down; 1-4-bit control; 2-4-bit control latch; 3-2-bit control	0-Power Down; 1-CKREF 20Mhz to 40MHz; 2-CKREF 5MHz to 14MHz; 3-CKREF 8MHz to 28MHz	0-Power Down; 1-CKREF 2Mhz to 5MHz; 2-CKREF 5MHz to 15MHz; 3-CKREF 10MHz to 26MHz	Master/slave; PAR/SPI; Strobe selection; Reset/standby; Slew control

µSerDes™ Family Similarities and Features

Similarities across FIN24AC, FIN224AC, and FIN224C

- Same Package
- Same Pinout
- Same Voltage Range
- Same Voltage Translation Range
- Same CTL Drive

New Features

- Rolled LVCMOS Deserializer Edge Rates
- More ESD Protection
- More Wide CKP Pulse Width (FIN224AC)
- Less Power (FIN224AC)

Implementation

What distance can a µSerDes™ drive?

The distance that can be driven depends on the data rates involved, acceptable bit error rate, and the transmission medium. The maximum distance in ANSI/TIA/EIA-644-A, the LVDS standard, is 10 meters. This distance is entirely application dependent.

Should special transmission mediums be used?

The µSerDes can be used with any typical differential transmission medium, including flex circuits, PC board, and cables.

What impedance should the transmission cable/flex be?

The transmission line should be 100Ω differential.

Is a termination resistor needed at the inputs to the deserializer?

No. The 100Ω termination resistor is integrated into the deserializer, so an external resistor is not necessary for either clock or data lines.

Do trace lengths need to be matched?

Yes. Trace lengths need to be matched like any bus architecture. However, since the serializer and deserializer have a flow-through design (traces do not need to cross to connect devices), the effort to achieve this is minimal.

Are there PCB layout guidelines available?

Yes. This can be downloaded from the Fairchild website or may be obtained from interface@fairchildsemi.com

What is the typical common-mode voltage of the µSerDes™?

Typical common-mode voltage is approximately 700mV.

Are there actual Gerber files available to download to simplify or as an example of design?

Yes, please contact Fairchild Interface Group at interface@fairchildsemi.com.

Is there a special power-down sequence between serializer and deserializer?

There is no required power-down sequence.

Is there a special power-up sequence between supplies for either a serializer or deserializer?

There is no required power-up sequence for either serializer or deserializer.

Are there special settings or switches for the PLL (S1, S2) on the FIN24 serializer?

No. The PLL has a very wide range of operation.

When is CTL™ technology better than single-ended, current-mode technology?

In applications where a transmission line must be AC coupled or when DC line balancing is necessary, single-ended, current-mode technology is usually inadequate. LVDS is superior because DC bias can be restored on the deserializer side of the solution by using only resistors. In addition, differential technologies offer better EMI than single-ended technologies.

How much is EMI reduced using a µSerDes™?

µSerDes provides ultra-low EMI as compared to legacy single-ended technologies. The actual amount of EMI reduction varies per application; however, Fairchild's EMI lab has documented cases of greater than -106.1dB reduction over legacy single-ended technologies.

Is there special grounding scheme required for µSerDes™?

No special ground wire is required. The ground wire can be subject to interference, as with single-ended, current-mode technologies.

How low is the power in power-down mode?

The µSerDes device is specified to use less than 10µA in power-down mode.

Are EMI filters necessary on the serial link?

Many applications no longer require EMI filters. If additional filtering is required, Fairchild suggests implementing a shielded flex of ribbon cable for the following reasons:

- Saves space on the PCB.
- Makes a solid ground between board assemblies (no ground bounce).
- Sideband signals in flex, not through µSerDes, can radiate; shielding helps reduce this phenomenon.
- ESD/EMI arrays are expensive.

Test and Diagnostics

Bits 21 and 22 on the FIN24A don't seem to work on the deserializer. Why?

Data input to pin 21 on the FIN24A serializer is output from the deserializer on pin 23. Data input to pin 22 on the FIN24A serializer is output at the deserializer on pin 24.

Why does the serial clock appear intermittent?

This is normal as a word boundary is embedded into the serial stream. Please refer to the datasheet for a more in-depth description.

When I examine either the serial data path or the serial clock path, the signal is distorted. Why?

Using a 50Ω high-speed terminated oscilloscope with the probe ground to one side of an LVDS signal forces the 1.0V bias to ground, resulting in a very incorrect signal. Use high-impedance probes or, alternatively, a board ground may be offset to accommodate the ground of an oscilloscope. Contact a Fairchild µSerDes representative for assistance.

How should the serial clock or data stream look?

The clock or data stream is approximately a 225mV peak-to-peak, roughly square, wave differential signal at approximately 700mV bias with respect to ground.

Where is the ground for µSerDes™ devices?

All device grounds are connected to the ground slug, underneath the µSerDes device. Care should be taken when designing the board containing the µSerDes so that the solder mask is pulled back from this slug.

Do S1 and S2 control the frequency range for the FIN24?

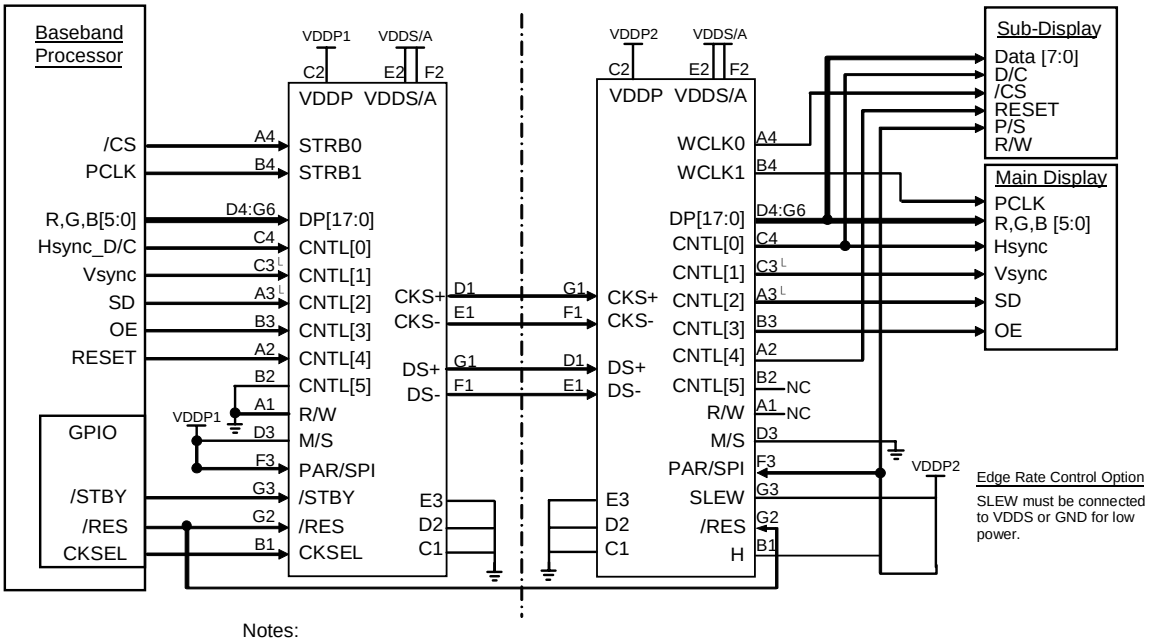
The FIN24 has a set frequency range, where S1 and S2 control the directionality of data bits [21:24].

What does a typical implementation look like for an RGB interface?

Please see Figure 1 for a typical implementation.

Where can I get more information on how to use a µSerDes™ with more complex architectures, such as microcontroller interface or for a bi-directional configuration?

Contact your local Fairchild representative or at interface@fairchildsemi.com.



Notes:
1. Write-only Interface.
2. Assumes BGA die on display.
3. /CS used to strobe sub-display data.
4. PCLK used for RGB mode.
5. Pin numbers for BGA package.

Figure 1. FIN324C RBG Application Example

Related Datasheets

FIN12AC
FIN12AC
FIN24AC
FIN24C
FIN224AC
FIN224C
FIN324C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